In the Specification:

Please amend paragraph [0036] as follows:

For example, consider the case where the program event occurs along an edge of one of fingers 26. Current traveling from gate contact 16 to diffusion/well contact 18 would encounter low resistance as it passed along gate conductor 12 and as it dropped down a substantially vertical portion of the current path from gate conductor 12 to active area 14 at the location of the programming event. The current would then encounter high resistance only where it traveled underneath a finger 26, because only in those locations would the current travel through high-resistivity N-diffusion. Everywhere else the current would encounter low-resistivity N+ implant. FIGS. 5 and 5A depict a MOS device 10 in which gate conductor 12 has been provided with fingers 26 and active area 14 has been provided with fingers 22 so as to again increase the length of intersection perimeter 20. As is true in the preceding figures, the heavy dark lines indicate regions of intersection perimeter 20, though in FIG. 5A, not all such regions have been marked with reference numerals. <u>One of said fingers 26 and said fingers 22 may have a width substantially equal to a minimum feature size.</u>

B1

OK